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(54) Control of power transfer in a flyback converter by modulating the off-phase in function of the load

(57) A method of controlling a flyback DC-DC converter, self-oscillating at steady state conditions, employing a transformer for storing and transferring energy to a load and having an auxiliary winding whose voltage, induced by the current flowing in the secondary winding of the transformer, is monitored to regulate the amount of energy being transferred by way of a primary control loop disabling and enabling the turning on of a power switch driving the primary winding of the transformer and to detect its the zero-crossing and consequently turn on the power switch for a new conduction and energy storage phase, the duration (T_{ON}) of which is established by a secondary control loop of the output voltage producing the turning off of the power switch for a new off phase (T_{OFF}), and comprising a fixed frequency oscillator of a frequency lower than the self-oscillating frequency of the converter for start-up charge transient of an output filter capacitor, wherein the power transferred from the primary circuit to the secondary circuit of the flyback transformer is controlled by introducing a delay on the turn-on instant of the power switch in respect to a turn-on command generated, during a self-oscillating functioning phase upon sensing a zero crossing event and during a fixed frequency functioning phase, upon a rising front of the signal generated by said oscillator, in function of input variables of the enabling-disabling primary control loop and of the secondary control loop, regardless of the mode of control.

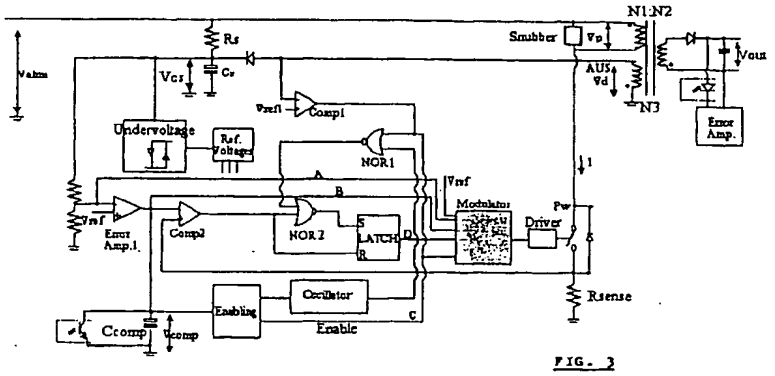

FIG. 3

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Description

FIELD OF APPLICATION OF THE INVENTION

[0001] The invention relates to flyback DC-DC converters.

TECHNOLOGICAL BACKGROUND

[0002] Intense research and development efforts are being done for improving and making even more adaptable to different important sectors of application integrated power supplies based on the use of DC-DC converters. Indeed, these power supplies, besides a high performance in terms of response to load transients and broad stability range, provide for an excellent static and dynamic behavior, in line with rules on containment of electromagnetic pollution, etc..

[0003] Particularly in VCR, TV, receivers and satellite decoders and similar consumer products, the quest is of minimizing the inventory of circuit components for reducing the cost of these appliances.

[0004] In recent years, many specially designed devices have been produced and marketed to serve these economically important applications. World leader manufacturers of electronic components such as STMicroelectronics market a wide spectrum range of monolithically integrated and hybrid devices designed to handle output powers of 30 to 300 W.

[0005] Yet, ever stricter requisites imposed on such integrated devices and enactment of severe specifications of the performances, often requires a substantially customization of the product in order to simplify layouts and reduce the number of components necessary to realize the power supply and costs.

[0006] In a broad range of consumer products, the configuration most frequently used is that of a so-called flyback self-oscillating power supply (SOPS).

[0007] A typical flyback scheme is shown in Fig. 1. This basic scheme of DC-DC converter circuit provides for a good control of power transfer with a switching frequency in the vicinity of about 100 kHz, requires the use of a relatively small flyback transformer and ensures a high efficiency in transferring power from the primary circuit to the secondary or output circuit.

[0008] Generally, in a SOPS converter a variable frequency control is implemented wherein the conduction phase (T_{ON}) of the power switch that drives the primary winding (phase of energy storing in the flyback transformer) is limited, as in a PWM system, by the maximum current and by the output voltage error, while the duration of the phase of nonconduction (T_{OFF}) (phase of transfer of the stored energy to the load connected to the output) is determined by the applied load.

[0009] To this purpose, the zero-cross event of the voltage induced by the current flowing in the secondary winding on a third or auxiliary winding is detected and a consequent logic signal of acknowledgment of the occurrence of such a zero-cross event turns on the power switch and starts a new conduction phase.

[0010] Fig. 2 shows the scheme of a flyback SOPS produced and marketed by SANKEN, in which the auxiliary winding AUX is exploited to power the control circuits of the converter.

[0011] By way of a delay network Tdelay, that is commonly realized with external discrete components, the switchings of the comparator C2 are synchronized with the null voltage condition on the current terminals of the power switch, in order to turn on the power switch in a condition of quasi-resonance so to avoid a classic flyback hard switching mode of operation of the converter.

[0012] The SOPS control, intrinsically a variable frequency type of control, forces the flyback converter to function close to the limit between a discontinuous mode (zeroing of the current in the primary during an off phase) and a continuous mode wherein in the primary winding a current continues to flow during an off phase of the power switch.

[0013] The (secondary) control loop, composed of the output voltage error amplifier ERROR AMPLIFIER, whose output is photocoupled by way of a photodiode and a phototransistor to the inputs of the comparators COMP1 and COMP2, the RC OSC network and the OSC block, intervenes to control the variations of the output voltage Vout, that occurs in function of the transfer of energy stored in the flyback transformer to the load. Therefore it is unable to handle the start-up phase, that is the charging transient of the whole capacitance coupled to the converter output.

[0014] This inability is commonly overcome by implementing another (primary) control loop by way of the comparator COMP1, the block ENABLING CIRCUITS and the logic AND gate and using a fixed frequency oscillator OSC, enabled by said other primary control loop, to turn on the power switch $P\omega$ with the rising front of a fixed frequency clock signal provided by the OSC oscillator, so to permit the start-up of the flyback converter until it reaches an output voltage sufficiently high to cause the passage to a proper self oscillating mode of operation.

[0015] In practice, during the start-up phase, the OSC oscillator imposes an off phase (T_{OFF}) of fixed duration, according to a Pulse Ratio Control (PRC) mode of operation.

[0016] Commonly, the OSC oscillator frequency is set by the RC-OSC network that is made of external components, to a value lower than the self-oscillating frequency of the flyback converter during its steady state functioning. This ensures, at a steady state, a discontinuous mode of a self-oscillating converter (SOPS), which is intrinsically a most controllable mode of operation..

[0017] Normally, in a SOPS system, when the load applied to the output decreases the switching frequency increases and this increments the losses due to the

switchings of the power switch.

[0018] Moreover, the unavoidable delays of the secondary control loop during the self-oscillating steady state functioning of the SOPS and the turn-off times typical of DMOS transistors, commonly used as power switches, dictate a minimum turn-on time (T_{ON}) of the converter and therefore a certain minimum quantity of stored energy in the transformer during each turn-on phase. This energy is totally transferred to the load. If the load absorbs an amount of energy lower than said certain minimum which is any case transferred, the output filter capacitor overcharges and therefore the output voltage Vout increases.

[0019] In these circumstances, the control system may only intervene by turning off the converter. This is done by disabling by way of dedicated ENABLING CIRCUITS the turning on of the Pω switch until the Vout drops below than a certain threshold. This determines a so-called burst mode of functioning, during which the SOPS converter functions by alternating periods of normal functioning with periods in which the switch is kept off.

[0020] Due to inevitable delays and to the turn-off time of the power transistor, SOPS are not suitable to supply relatively small loads and/or for prolonged stand-by conditions. For these applications, a control system capable of limiting the power transferred to the output in a more effective way such as for example a fixed frequency control, is commonly preferred.

[0021] Normally, in many applications, when the load is reduced to stand-by conditions, a fixed frequency mode of control is enabled, in order to facilitate the control and reduce losses.

[0022] The consequent decrease of the energy transferred to the output, and the limitation of the overshoot of the output voltage may indeed reestablish the conditions for a transition to an variable frequency SOPS control mode which in turn may cause a new overshoot of the output voltage. The converter may then "oscillate" between two modes of control: the variable frequency SOPS control and the fixed frequency control (at the frequency of the start-up and recovery oscillator).

[0023] Under these conditions, the current supplied by the error amplifier of the output voltage and consequently the current that flows in the power switch take a wavyform, that is they present a sequence of peaks and lows.

[0024] A similar behavior may be observed when the load of the converter is subject to an abrupt stepwise drop. Even in this case, the abrupt discontinuity of the load level induces a marked overshoot followed by an undulatory decay pattern of the current profiles of the error amplifier and of the power switch.

[0025] These behaviors as well as a burst mode of operation cause inefficiencies and remarkably increase the electromagnetic noise produced by the converter.

OBJECT AND SUMMARY OF THE INVENTION

[0026] A solution to the above noted drawbacks and limitations of known SOPS systems has now been found. Apart from markedly attenuating the undulatory decaying of currents following an abrupt reduction of the load and averting repeated transitions from a self-oscillating mode to a fixed frequency mode of operation of the converter, the present invention practically prevents a burst mode of functioning of the converter.

[0027] This important result is obtained, according to the present invention, by controlling the power transferred through the flyback transformer, by modulating the duration of the off phase of the power switch in function of a combination of current operation parameters of the converter in order to maintain the converter in a SOPS functioning mode until reaching limit output voltage conditions such to determine the transition from a self-oscillating mode to a fixed oscillator frequency mode. On one hand, this prevents an intermittent or burst mode functioning of the converter and on the other hand this limits the voltage overshoot phenomena and the consequent decay transients upon a transition from a SOPS control to a fixed frequency control and/or abrupt reduction of the load (stand-by).

[0028] According to a preferred embodiment of the invention, the modulation of the duration of the off phase of the power switch while substantially preserving a SOPS functioning mode of the converter, is implemented by adding a circuit block that modulates the off interval suitably coupled between the output of the bistable control circuit and the driver stage of the power transistor of the converter.

[0029] Fundamentally, the approach of the invention is to introduce a modulation of the amount of energy transferred to the output by forcing the converter, during control transients and its steady state functioning, to operate in a more or less discontinuous manner compared to a limit condition of self-oscillating mode, thus introducing an effective modulation of the gain of the converter in function of the applied load.

[0030] This is done by controlling the off interval which, while leaving the converter functioning in a SOPS mode, makes it to function in a so-called PRC mode, whereby the off interval is determined by input parameter signals of the control system of the converter.

[0031] A modulation of the energy transfer is obtained that even under low load conditions, stabilizes the functioning of the converter, practically eliminating the burst mode and limiting the overshoot at transitions between self-oscillating mode and fixed frequency mode.

[0032] The discontinuity represented by this transition between the two functioning modes (self-oscillating and fixed frequency) is more efficiently handled by such a modulation that acts for maintaining constant the output voltage.

[0033] Moreover, by acting directly upon the energy transfer and limiting the overshoots a notable increment of the fastness of response of the converter is observed.

[0034] The invention is more clearly defined in the appended claims 1 and 3 and particularly preferred embodiments are defined in the dependent subsequent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035]

Figure 1 is a basic scheme of a flyback DC-DC converter.

Figure 2 is a comprehensive diagram of a flyback SOPS.

Figure 3 is a diagram of a flyback SOPS converter made according to the present invention.

Figure 4 is a detailed diagram of the modulating block of the diagram of Fig. 3.

Figure 5 shows the waveforms of the significant signals of a converter of Fig. 3.

Figures 6, 7 and 8 show the waveform of the significant signals, including the response to a step-wise variation of the load converter shown in Fig. 3, with and without the modulating block of the invention.

DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

[0036] The embodiment shown in Fig. 3 is one among possible forms of realization the proposed invention. It relates to a flyback converter destined to function in two modes:

a) at a fixed frequency normally of a low value (around 16÷20 kHz); this functioning mode is automatically commanded by the control circuit when a relatively low output power is required, such as for example during a stand-by condition of TV sets or VCRs;

b) in a self-oscillating SOPS mode when under nominal power conditions of operation of the converter. Even this functioning mode is automatically commanded by the control circuit. The latter functioning mode does not represent the only condition in which the invention may be advantageously implemented by way of introducing a modulation of the duty cycle, indeed the invention remains effective also during a phase of operation at frequency using a switching frequency between 100 and 200 Khz for reaching up to the maximum level of power transfer to the load.

[0037] For an architecture as that shown in Fig. 3, the start-up and the recovery phases are managed by the circuit UNDERVOLTAGE, similarly to known architectures. Such a circuit disables the voltage sources of the block REF. VOLTAGES until reaching a positive threshold Vcs(H). Thereby, it is possible to charge the supply capacitor Cs with a low current which may be supplied, as shown in Fig. 3, through a resistor Rs of adequate value and dissipation characteristics. Otherwise an initial charging of Cs may be arranged through an integrated network.

[0038] Once the threshold Vcs(H) is reached, the UNDERVOLTAGE circuit enables, with a certain hysteresis the control circuits of the converter. This discharges the capacitor Cs. If the voltage on the Cs terminals drops below a positive threshold Vcs(L), lower than Vcs(H), the UNDERVOLTAGE circuit will disable again the powering of the control circuitry, allowing for a recharging of the Cs capacitor. The electric charge stored in Cs is sufficient to ensure the completion of several switching cycles of the converter and therefore an energy transfer to the output and to the auxiliary circuits.

[0039] Under steady state conditions, the voltage Vcs is kept higher than the Vcs(L) threshold by the current delivered by the auxiliary winding AUS during an OFF phase of the power switch, which, in Fig. 3 is represented by a switch driven by the stage DRIVER.

[0040] The output voltage Vout is controlled by two different control loops.

1) Primary control loop
The primary loop controls, by means of a voltage divider and an error amplifier ERROR AMP1 having its inverting input (-) coupled to a tap of the voltage divider, the Vcs voltage of self-powering of the control circuitry. Such a voltage Vcs is tied to the output voltage Vout by the turn ratio N2:N3 of the transformer, thereby depending on the characteristics of the transformer. The primary control loop does not have a high precision, but it has the advantage of not requiring external circuits.

2) Secondary control loop
The secondary loop directly controls the output voltage Vout by means of an error amplifier ERROR AMP and an optocoupling to the VCOMP pin of the integrated control circuitry of the converter thus ensuring electrical isolation of the DC output voltage of the converter from the circuits linked to the VALIM supply voltage (rectified mains voltage).
Such a control provides for a high precision. For this reason it is implemented in a large number of applications even though it requires the use of external components and has a higher cost.

[0041] For both modes, compensation of the control loop is provided by a CCOMP capacitor, generally connected externally.

[0042] Through the comparator COMP2, the VCOMP voltage present on the compensation capacitor CCOMP controls the turn-off of the power switch according to the following formula:

VCOMP = RSENSE*1

[0043] This occurs by enabling a logic state "1" on the reset R of the bistable circuit LATCH.

[0044] The logic gate NOR2 guarantees the predominance of the reset signal R on the set signal S in order to avert a possible condition of indetermination.

[0045] In self-oscillating converters the switching frequency of the converter is variable and depends on the applied load.

[0046] The turn-off phase of the power switch, OFF phase, lasts until a complete transfer to the output circuit of the energy stored in the transformer during the preceding conducting phase of the power switch, ON phase, has occurred.

[0047] Once this transfer is completed, the voltages at the terminals of the transformer tend to nullify themselves.

[0048] In known converters such a tendency is exploited to command the turning on of the power switch and the beginning of a new, ON phase, to store energy in the transformer. The energy stored in the primary winding inductance L1 of the transformer during the ON phase is given by:

$$\frac{L_1 I^2}{2}$$

and the output power, being the energy stored totally transferred, is :

$$\eta * \frac{L_1 I^2 f}{2}$$

where η is the efficiency of the converter and f is the switching frequency that is determined by the load conditions.

[0049] The less is the applied load the higher is f, because both the ON phase and the OFF phase are short in view of the fact that the load requires less power.

[0050] The minimum switch-off and switch-on time intervals of the power switch are imposed by the geometry of the device. This implies that even for very low loads or under stand-by conditions, a minimum storage of energy occurs in the transformer, energy that is eventually transferred to the load during the OFF phase.

[0051] If the load absorbs less than this minimum energy transfer, the self-oscillating converter enters into a "Burst Mode" of operation characterized by few active switching cycles that cause an overshoot of the output voltage are followed by an interval of time during which switching-on of the power switch is disabled (VCOMP voltage made null) until the overshoot of the output voltage has decayed.

[0052] If the load absorbs required a power lower than the power dissipated by the control circuitry of the converter, a functioning mode referred to as "Bad Burst Mode" may take place, in which the turn-off interval of the power switch becomes so long as to discharge the Cs capacitance which continues to power the integrated circuitry to a voltage below the Vcs(L) threshold, thus imposing a new start-up and recovery phase.

[0053] The present invention permits to establish automatically a fixed frequency functioning mode for low loads and a self-oscillating functioning mode that substantially prevents either a Bad Burst Mode and even a Burst Mode.

[0054] An excess voltage condition at the output of the converter is reported by the above described feedback loops in form of a decrease of the VCOMP voltage. Under a certain threshold, the ENABLING block activates, according to the present invention, the fixed frequency functioning mode.

[0055] During the initial start-up phase and/or a recovery phase of the device, the CCOMP capacitor is discharged in a substantially state and the voltage VCOMP on its terminals is approximately zero; this determines that the initial functioning mode of the converter be at a fixed frequency.

[0056] During this fixed frequency functioning mode, the ENABLE signal is placed to a logic level "0", thus determining through the logic operator NOR1 the predominance of the signal generated by the block OSCILLATOR.

[0057] During the OFF phase, being the power switch "open", the COMP2 output places to a logic level "0" the reset "R" of the bistable circuit LATCH, while the rising front of the fixed frequency signal generated by the block OSCILLATOR imposes a logic level "1" to the set "S" of the LATCH which brings its output to a logic level "1". In this functioning mode such a logic level causes (through the MODULATOR block and the DRIVER block) the "closing" of the power switch and the beginning of a successive ON phase.

[0058] During a self-oscillating functioning mode, the ENABLING block imposes a logic level "1" to the ENABLE signal and disables the OSCILLATOR block which brings its output to a logic "0". This determines the predominance of the signa output by the COMP1 comparator through the logic operator NOR1. At the instant the voltage on the transformer windings becomes null (that is, when completing the transfer to the output of the energy stored in the transformer during the preceding ON phase), the output of the COMP1 block is set to a logic level "1", determining, as during operation at a fixed frequency, the switch of the output of the bistable current LATCH to a logic level "1".

[0059] Without the MODULATOR block, such a condition would cause the turning on of power switch, even in this functioning mode.

[0060] In the preferred embodiment of the invention shown in Fig. 3, the MODULATOR block limits the overshoot of the output voltage as well as its effect by

speeding up the response of the converter to intervening load variations while permitting a correct and gradual transition between the two functioning modes.

[0061] The MODULATOR block may have a functional architecture as shown in Fig. 4. Its intervention is caused by the signal A which represents the Vcs (primary loop variable) and by the signal B which represents the VCOMP (secondary loop variable).

[0062] The other signals input to the MODULATOR block are:

- the C signal, that is, the signal that was already defined ENABLE in relation to the diagram of Fig. 3; its logic level "0" commands a fixed frequency functioning mode, its logic level "1" commands a self-oscillating functioning mode;
- the D signal, that is, the output of the bistable circuit LATCH of Fig. 3; its logic level "0" causes the turning-off of the power switch, its logic level "1" causes the immediate turning on of the power switch during a fixed frequency functioning mode. In a self-oscillating mode, the MODULATOR block introduces a delay on the switch-on signal (D=1) of the power switch of a magnitude that depends on the overvoltage condition of the output.

[0063] The two signals A and B are compared with respective references in the COMPA and COMPB blocks, the output of each of these two blocks is compared to a ramp signal synchronous with the D signal (power turn-on signal) in the COMPAA and COMPBB blocks, respectively.

[0064] The logic block OR allows for:

- enabling the MODULATOR block when the inverse of the signal C (obtained through the NOT gate) is at a logic level "0" , that is, the ENABLE signal is at level "1";
- operating a timewise modulation depending on the monitoring of more control variables (Vcs and VCOMP).

[0065] The output of the AND gate combining the output of the OR gate with the power switch turn-on signal D, drives the bistable circuit LATCH of Fig. 4, whose output controls the stage driver of the power switch.

[0066] The set signal is predominant in the LATCH circuit.

[0067] According to this invention, the modulation block MODULATOR may be advantageously introduced in power supplies with a duty cycle control.

[0068] The modulation block and related logics of the invention may be similarly used in control loops operating either in voltage mode or in the current mode.

[0069] Generally, such a time modulation block will be functionally introduced upstream of the actuators (driver stage and the like) and when it is enabled it will adequately delay the switching on of the power switch by an interval that is determined by the functioning condition, regardless of the type of control mode being currently used.

[0070] Should the load no longer absorb the entire energy transferred to the output in a SOPS system (which inevitably takes place in a start-up phase) the output voltage will increase causing the intervention of both the conventional control circuitry as well as the modulation block of the invention.

[0071] In this way, the transfer of energy to the output is reduced by effectively lowering the gain of the converter circuit, thus limiting the overshoot of the output voltage, whereas the conventional control circuitry, because of nonnegligible response times, would lead to substantial overshoots.

[0072] This combination of effects of the conventional control system and of the auxiliary time modulation of the invention, outstandingly stabilizes the output voltage and cause a gradual disabling of the modulation block of the invention allowing on one hand the fullest transfer of energy while on the other hand limiting overshoots.

[0073] The output voltage Vout is kept within a restricted range thanks to the action of the modulation block of the invention. The control circuit of the converter, by coming out of an overshoot through a markedly damped oscillations, due to the output capacitance and to the characteristics of the output voltage error amplifier, quickly stabilizes to the new steady state condition.

[0074] Indeed, the initial overshoot that occurs with a traditional control circuit allows to stabilize the converter of the invention in case of relatively low loads.

[0075] During stand-by conditions, that is, for load levels that cannot not be stably supplied in a self-oscillating mode (for the reasons already described above), the converter automatically passes to function in a fixed frequency mode.

[0076] Even in this situation, where the converter may temporarily turn itself off because of the overshoot, the action of the modulator introduced according to the present invention stabilizes and keeps the output voltage within a small range during the entire transient.

[0077] According to the present invention:

a) a modulation of the energy transfer is introduced only in a phase of regulation, and therefore it acts on the transients making the converter overcome the noted drawbacks, thus extending the stability range regardless of the functioning mode with which the system reaches a steady state;

1) for the correct functioning of the modulation block, it is sufficient to exploit signals that are already used in a common control circuit of the converter without requiring additional external circuits and components;

2) the modulating action is undertaken by con-

trolling the T_{OFF} time, practically adding itself to the normal control of the time T_{ON}, thus overcoming exceeding the limits imposed by the presence of switching delays in the common control loop.

[0078] The following are some of the important advantages of the invention:

1) the modulation block may be easily introduced in the circuit architecture of a traditional control circuit and integrated with it;
2) the control on the energy transfer acts on the transfer function depending on the load conditions, compensating the negative effects of abrupt load variations without requiring the introduction of sensors of the current delivered to the load;
3) the invention may be applied to regulators having different functioning modes and/or of different type; in particular the architecture of the invention may be used to support the action of a FUZZY control replacing a traditional control circuit of the converter;
4) the limiting of the energy transfer operated by the modulator block of the invention takes place only during the transients, without affecting in any way the maximum steady state transfer allowed by the type of converter and relative control;
5) the discontinuity between the self-oscillating functioning mode and the fixed frequency functioning mode is substantially eliminated. This reduces in the electromagnetic noises produced by the converter;
6) the response speed of the converter is enhanced;
7) there is an extension of the self-oscillating functioning mode toward relatively lower levels of load, thus substantially preventing the burst mode and the bad burst mode;
8) the fixed frequency functioning at extremely low loads is outstandingly stable;
9) a combination of effects of the primary control loop (feedforward: variables referred to an auxiliary winding of the transformer) and of the secondary control loop (feedback: variables proportional to the output voltage) is advantageously implemented according to the invention.

[0079] The invention has been tested and simulated on a functional model realized in a SIMULINK environment. This has permitted the reproduction of the waveforms of the significant current and voltage signals and a comparison between the behaviors of the converter with and without the modulator of the invention.

[0080] Fig. 6 depicts the waveforms of the current output by the error amplifier of the output voltage and of the current through the power switch at start-up, with an applied load of about 40W under the control of the primary loop, of the flyback switching converter of in Fig. 3, in which the energy transfer modulator block MODULATOR of the invention had been introduced. For the same testing conditions, Fig. 7 shows the waveforms of the same signals without a modulator block of the invention.

[0081] Figures 8 and 9 show the waveforms of the same signals for a converter with and without the modulator block, respectively, these waveforms highlight the transient that occurs at start-up with a 200W load, until about 20ms, and upon a stepwise is reduction of the load to about 4W.

Claims

1. A method of controlling a flyback DC-DC converter, self-oscillating at steady state conditions, employing a transformer for storing and transferring energy to a load and having an auxiliary winding whose voltage, induced by the current flowing in the secondary winding of the transformer, is monitored to regulate the amount of energy being transferred by way of a primary control loop disabling and enabling the turning on of a power switch driving the primary winding of the transformer and to detect its the zero-crossing and consequently turn on the power switch for a new conduction and energy storage phase, the duration (T_{ON}) of which is established by a secondary control loop of the output voltage producing the turning off of the power switch for a new off phase (T_{OFF}), and comprising a fixed frequency oscillator of a frequency lower than the self-oscillating frequency of the converter for start-up charge transient of an output filter capacitor, characterized in that it comprises

   controlling the power transferred from the primary circuit to the secondary circuit of said flyback transformer is controlled by introducing a delay on the turn-on instant of said power switch in respect to a turn-on command generated, during a self-oscillating functioning phase upon sensing said zero crossing event and during a fixed frequency functioning phase, upon a rising front of the signal generated by said oscillator, in function of input variables of said enabling-disabling primary control loop and of said secondary control loop, regardless of the mode of control.

2. A DC-DC flyback converter self-oscillating under steady state conditions, employing a transformer (N1, N2, N3) for storing and transferring energy to a load and having an auxiliary winding (AUS) charging a supply capacitor (Cs) of a control circuit of the converter, hysteresis means (UNDER VOLTAGE) enabling the control circuit of the converter when the voltage (Vcs) on said supply capacitor (Cs) exceeds a certain threshold, an enabling/disabling

primary control loop of the turning-on of a power switch (Pω) driving the primary winding of said transformer, composed of a first error amplifier of the voltage (Vcs) on said supply capacitor in respect to a first reference voltage (Vref), a comparator (COMP2) of a voltage proportional to the current flowing said power switch (Pω) with the output of said error amplifier (ERROR AMP1), resetting a bistable circuit (LATCH) controlling a driving stage (DRIVER) of said power switch (Pω), a secondary control loop of the output voltage (Vout) comprising a second error amplifier (ERROR AMP) of the output voltage in respect to a fixed reference, means photocoupling the output of said error amplifier (ERROR AMP) to the input node of said comparator (COMP2) coupled to the output of said first error amplifier (ERROR AMP1) and a disabling-enabling circuit (ENABLING) of a fixed frequency (OSCILLATOR) of a frequency lower than the frequency of self-oscillation of the converter, a second comparator (COMP1) functionally connected to detect the zero crossing of the voltage (Vd) induced on said auxiliary winding (AUS) by the current flowing in the secondary winding of the transformer and combinatory logic means (NOR1, NOR2) imposing the predominance of the set signal of said bistable circuit (LATCH) over the signal output by said first comparator (COMP2) or over the signal output by the combinatory logic circuit (NOR1) of the signals output by said second comparator (COMP1) and/or by said oscillation (OSCILLATOR), characterized in that it further comprises

a block (MODULATOR) functionally interposed between the output (D) of said bistable circuit (LATCH) and to the input of said driver stage (DRIVER) for introducing a delay on the turn-on instant of said power switch (Pω) in respect to a turn-on command (D) output by said bistable circuit (LATCH), depending on an enabling state of the signal (C) generated by said circuit ENABLING and on the signal existing at the input of said first error amplifier (ERROR AMP1) and on its output node (VCOMP).

3. A DC-DC converter according to claim 2, characterized in that said block (MODULATOR) comprises

a first comparator (COMPA) of the voltage (A) present at the input of said first error amplifier (ERROR AMP1) with a reference voltage (Vref); a second comparator (COMPB) comparing the error voltage present at the output node of said first error amplifier (ERROR AMP1) with said reference voltage (Vref);
a ramp generator (Ramp. Gen.) activated by a turn-on command (D) produced at the output of said bistable circuit (LATCH);
a third comparator (COMPAA) comparing the output of said first comparator (COMPA) with the output of said ramp generator (Ramp. Gen.) and a fourth comparator (COMPBB) comparing the output of said second comparator (COMPB) with the output of said ramp generator (Ramp. Gen.);
a first logic gate (OR) having inputs coupled to the outputs of said third and fourth comparators and a third input coupled to the inverted signal (NOR) output by said circuit ENABLING;
an output bistable circuit (LATCH) having a set input (S) coupled to the output of a second logic gate (AND) having an input coupled to the output of said first logic gate (OR) and a second input coupled to said turn-on command (D) and a reset input (R) driven by the inverted output signal of said second logic gate (AND);
the output of said bistable circuit (LATCH) being coupled to the input of a driving stage (DRIVER) of the power switch (Pω).

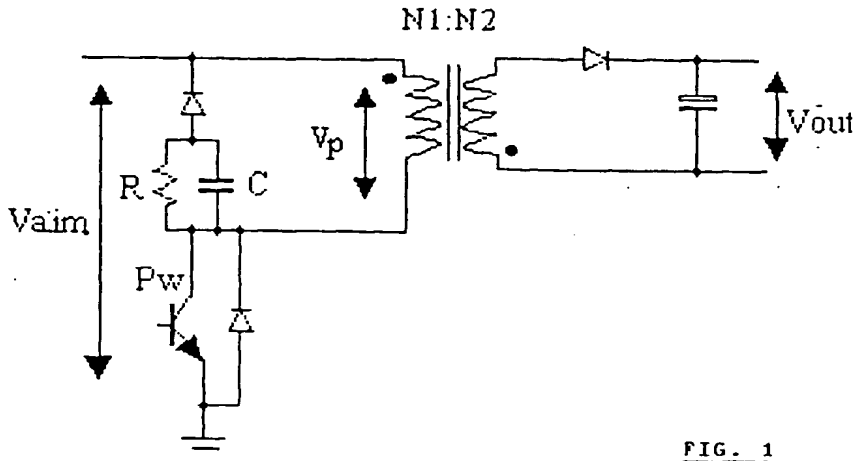
N1:N2
Vp
Vout
R
C
Vaim
Pw

FIG. 1

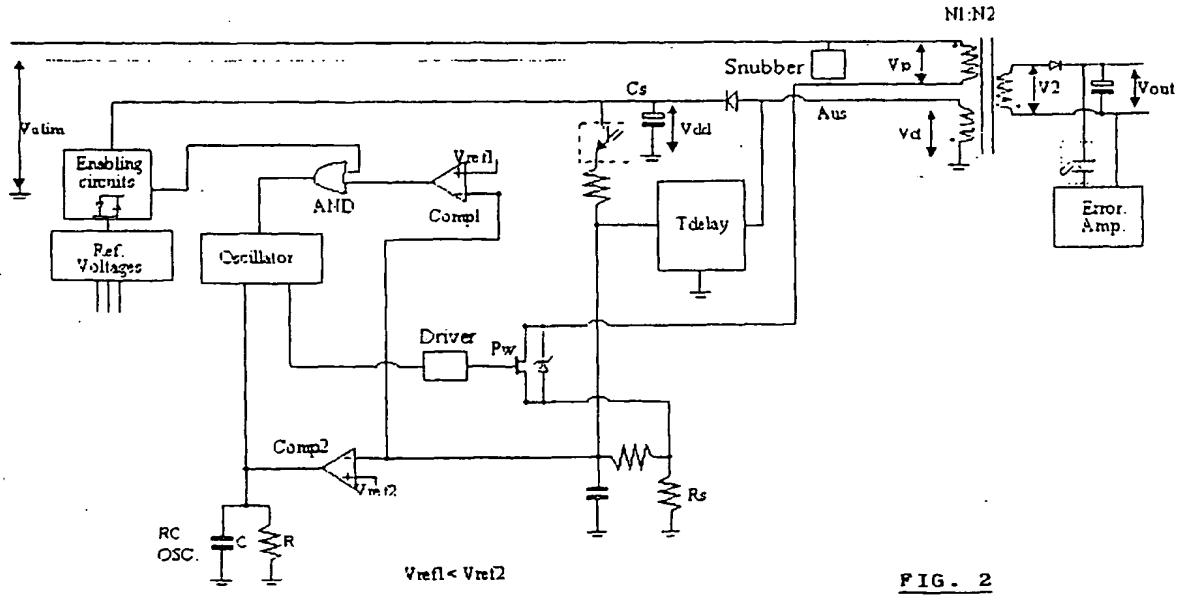
N1:N2
Snubber
Vp
Cs
Vout
V2
Vaim
Vdd
Aus
Vd
Enabling circuits
AND
Vref1
Compl
Tdelay
Error Amp.
Ref. Voltages
Oscillator
Driver
Pw
Comp2
Vref2
Rs
RC OSC.
C
R
Vref1< Vref2

FIG. 2

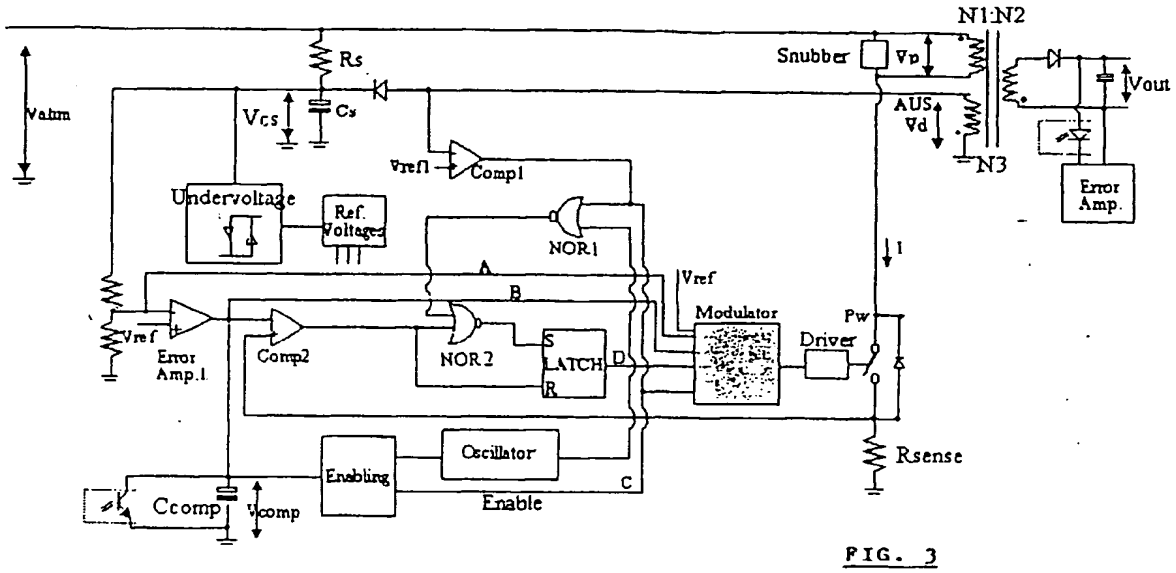
N1:N2
Rs
Snubber
Vp
Vout
Vaux
Vcs
Cs
AUS
Vd
N3
Error Amp.
Vref1
Comp1
Undervoltage
Ref. Voltage
NOR1
I
A
B
Vref
Modulator
Pw
Driver
Vref
Error Amp.1
Comp2
NOR2
S
LATCH
R
D
Rsense
Oscillator
Enabling
C
Enable
Ccomp
Vcomp

FIG. 3

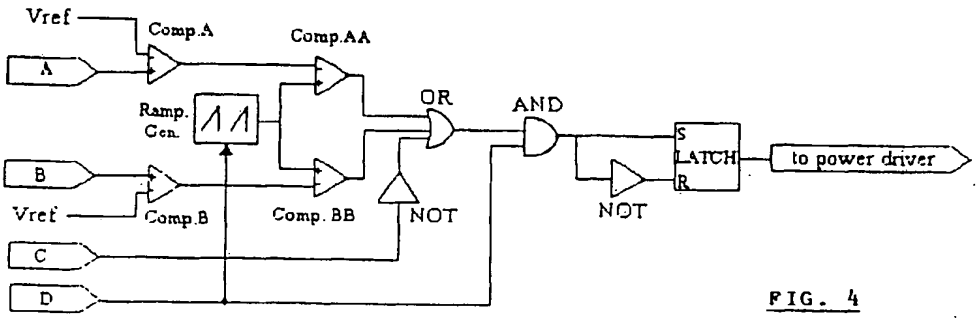
Vref
Comp.A
Comp.AA
A
Ramp. Gen.
OR
AND
S
LATCH
R
to power driver
B
Vref
Comp.B
Comp. BB
NOT
NOT
C
D

FIG. 4

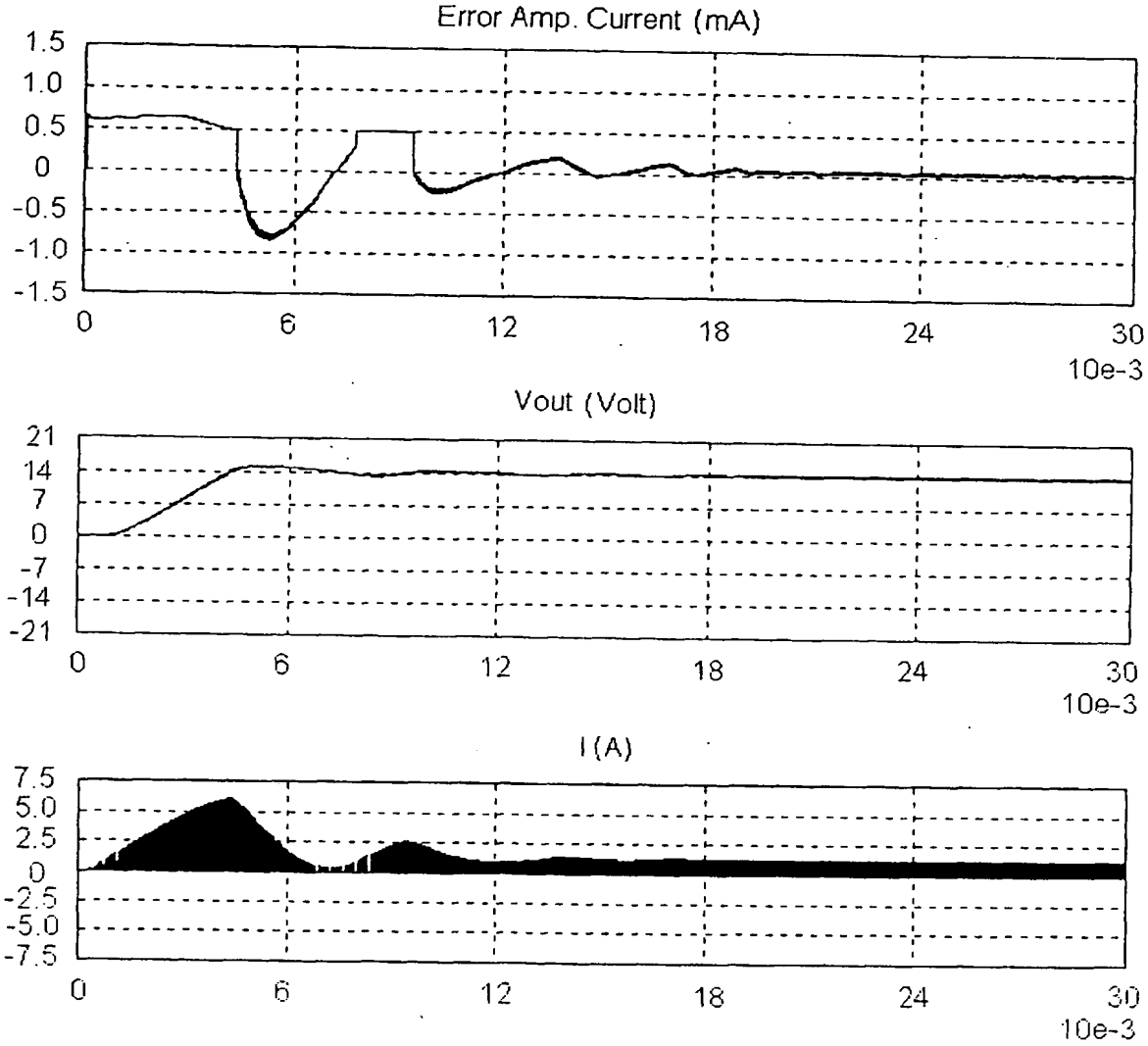

FIG. 5

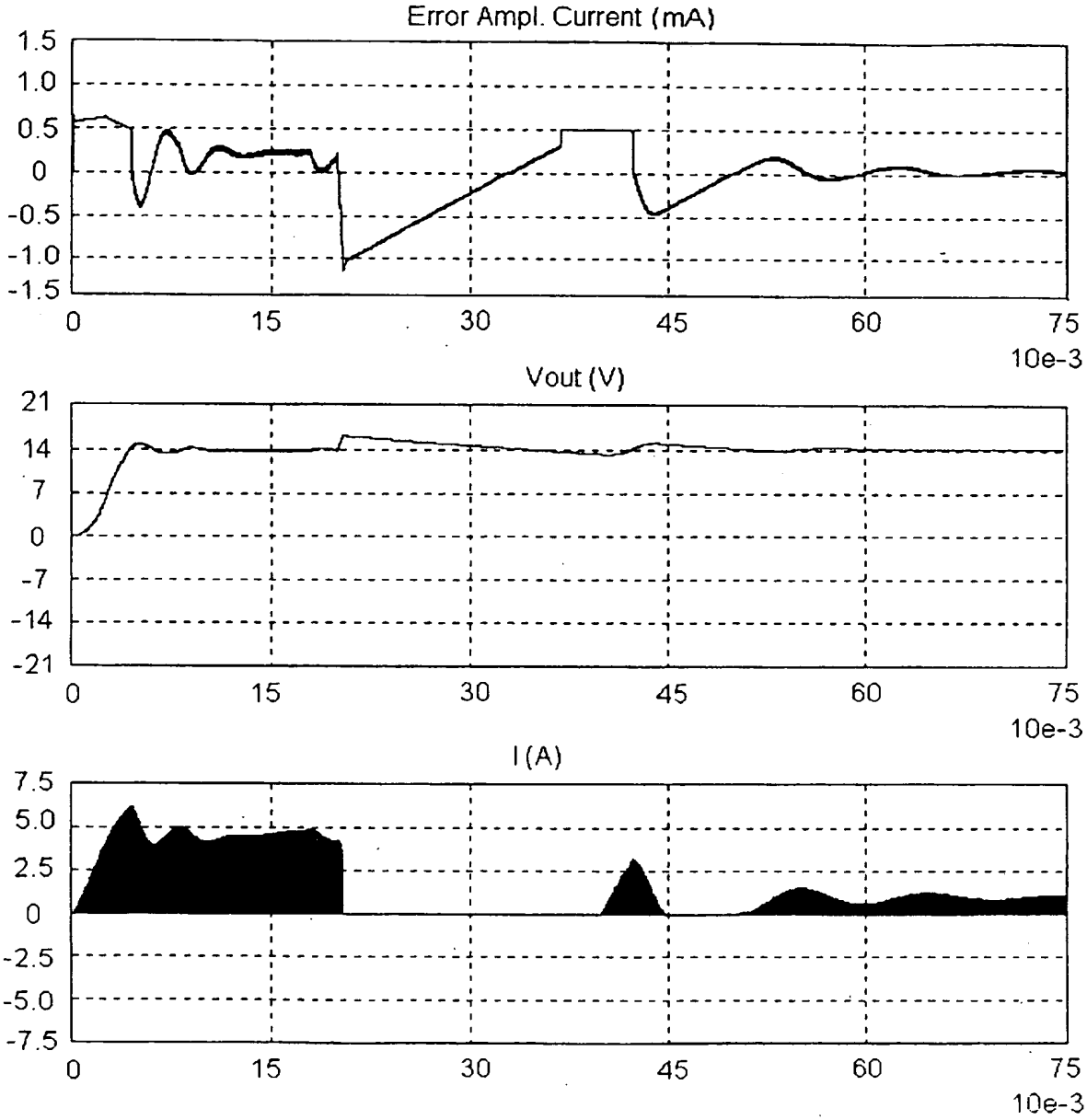
Error Ampl. Current (mA)
1.5
1.0
0.5
0
-0.5
-1.0
-1.5
0
15
30
45
60
75
10e-3
Vout (V)
21
14
7
0
-7
-14
-21
0
15
30
45
60
75
10e-3
I (A)
7.5
5.0
2.5
0
-2.5
-5.0
-7.5
0
15
30
45
60
75
10e-3

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0591

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 748 461 A (PRELLER PETER) 5 May 1998 * the whole document * ---	1,2	H02M3/335
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H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 February 1999	Thisse, S

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19-02-1999

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		JP 2231957 A	13-09-1990
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